*International Journal of Engineering Applied Sciences and Technology, 2022*
**Vol. 6, Issue 12, ISSN No. 2455-2143, Pages 241-246**
Published Online April 2022 in IJEAST (http://www.ijeast.com)

# ANALYTICAL MODELLING AND SIMULATION OF TRIPLE MATERIALS DOUBLE GATE GERMANIUM SOURCE FERROELECTRIC TUNNEL FET FOR LOW POWER APPLICATIONS

Joel M, Hemanth L K, G Ratandeep, K Lokesh
Undergraduate student
B.Tech Electronics and Communication Engineering
Reva University, Bangalore, Karnataka

***Abstract*** **- At the nanoscale, many multigate devices are being studied in order to reduce their size and improve their performance. This paper describes the design and development of a novel device known as the Triple Material Surrounding Gate Tunnel Field Effect Transistor (TMSGTFET). The advantages of encircling gate and tunnel FET are combined to build a novel structure. The gate material around the device is replaced with three gate materials with various work functions to prevent short channel effects. The device's surface potential, lateral electric field, vertical electric field, and drain current are all modelled in two dimensions, with the results explained. By altering the thickness of the ferroelectric layer and ferroelectric material, as well as verifying the simulation findings with MATLAB, we study the impacts of device parameters on the channel potential and on-state current.**
**The findings show that raising the ferroelectric layer thickness enhances the device's characteristics by reducing the shortest tunnelling length. Furthermore, the proposed analytical model shows increased ON current. CAD simulation is used to test the model's improved device properties, confirming that it is accurate.**

***Keywords***- **Ferroelectric Layer, tunnel field effect transistor, analytical model**

## I. INTRODUCTION

Semiconductor electronics are rapidly improving in terms of performance and complexity. This remarkable advancement is the consequence of continuous downscaling of MOSFET technology, which is necessary to meet the requirements for speed, complexity, circuit density, and power consumption. Many new unique nanostructures are introduced as a result of device downscaling, ensuring high functionality, high device drive, and low power consumption, all of which are critical factors in the evolution of electronics. Short channel effects (SCEs) are unwanted effects that occur as the channel length shorten, reducing device performance. As a result, research into SCEs is critical, as they pose a serious threat to efforts to downscale MOS technology. When the continual shrinking of MOSFET feature sizes reaches fundamental performance limits, new devices that use tunnelling for their ON-current must be investigated. The Tunnel FET, which can be used to replace standard MOSFETs in low-power applications, is onesuch promising device. In a circuit, a TFET can replace a MOSFET and has the following advantages: low leakage current in the femtoampere range and subthreshold swing < 60mV/dec.
Physical models are important to device engineers because they define the relationship between the device's electrical characteristics and physical parameters, as is well known. As a result, it's necessary to create an analytical model for double gate TFETs so that device properties can be improved while the structure is optimized. By merging the pseudo two- dimensional (2D) Poisson's equation with Maxwell's equation, the model is formed. Although the model did not take into account the device's 2D effects, an analytical drain current model for a vertical double-gate TFET was developed. However, 2D effects must be considered in nanoscale devices.

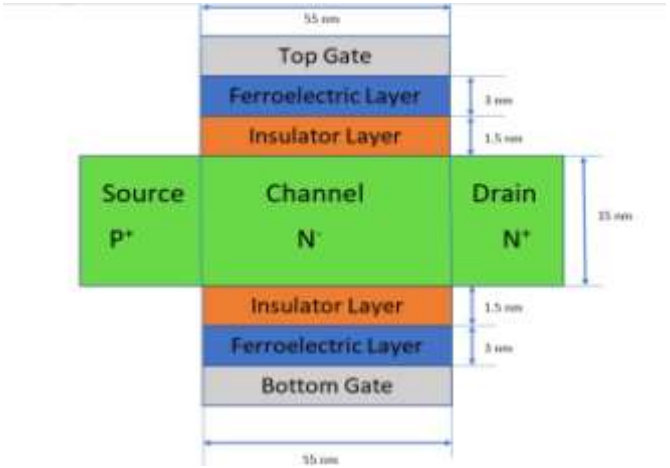



Fig.1. (Color online) Structure of the DG TFETs witha metal–FE–insulator–semiconductor

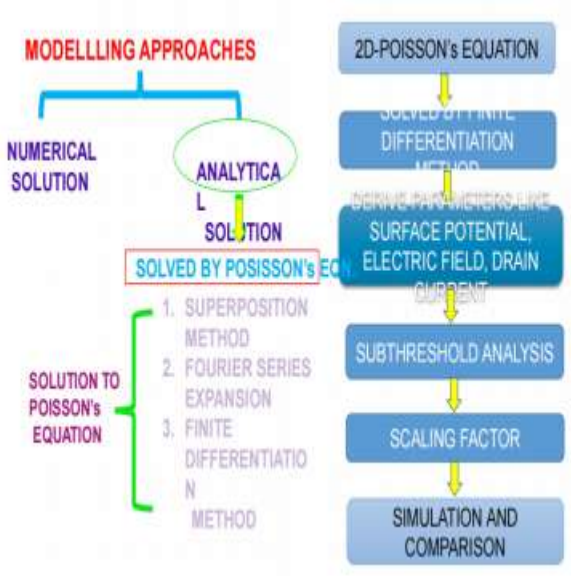
*International Journal of Engineering Applied Sciences and Technology, 2022*
**Vol. 6, Issue 12, ISSN No. 2455-2143, Pages 241-246**
Published Online April 2022 in IJEAST (http://www.ijeast.com)

To overcome the flaws of the previous models, an analytical model for double gate TFETs with ferroelectric layer is created. The nonlinear Poisson's equation is solved with the Landau–Kalashnikov (LK) equation to give the channel potential profile. The surface potential profile can be used to calculate the lateral and vertical electric fields. Kane's model can be used to calculate the drain current.

## II. DEVICE STRUCTURE AND NUMERICAL SIMULATION METHOD

Figure 1 shows the cross-sectional schematics of the proposed double gate TFETs. The channel's length L is 55 nm. The silicon film's thickness is ts, and its value is 15 nm. The insulator layer is tin and has a thickness of 1.5 nm. tf represents the thickness of the ferroelectric layer. The channel is intrinsic ($N_{CH}$ =$10^{16}$ $cm^3$), with the p+ source region doped at $10^{20}$ $cm^3$ ($N_S$) and the n+ drain region doped at 6*$10^{18}$ $cm^3$ ($N_S$) ($N_D$). The x-axis is perpendicular to the channel's direction, while the y-axis is parallel to it. The origin of the coordinate axis is at the middle of the source-channel region boundary.

The simulated findings for NC DG TFETs with a metal–FE– insulator–semiconductor (MFIS) structure cannot be obtained directly due to the lack of a corresponding exact FE polarization model. A metal–FE–metal–insulator–semiconductor (MFMIS) structure is used to replace the MFIS structure. Device parameters of double gate TFETs may be computed using the Silvaco Atlas TCAD device simulator anda one-dimensional (1D) LK equation.




## III. ANALYTICAL MODEL

**Calculation of potential distribution**

Because doping concentrations are relatively high in these regions, the voltage drop across the source and drain regions can be neglected.

The 2D Poisson equation is used to solve the channel potentialφ(x, y)

$$\frac{\partial^2\varphi(x,y)}{\partial x^2}+\frac{\partial^2\varphi(x,y)}{\partial y^2}=\frac{q}{\varepsilon_{si}}n_i\exp\left[\frac{\varphi(x,y)-V}{V_t}\right], \quad (1)$$

where q represents the electronic charge, εsi represents the silicon permittivity, ni represents the intrinsic carrier density, Vrepresents the electron quasi-Fermi potential, and is the thermal voltage.

φ(x,y) is decomposed into a 1D and 2D component along thechannel depth direction (y) and expressed as

$$\varphi(x,y)=\varphi_0(y)+\varphi_1(x,y). \quad (2)$$

Using the LK equation, the charge–voltage characteristic of the ferroelectric material is expressed as

$$V_f=a_0Q+b_0Q^3+c_0Q^5, \quad (3)$$

The FE layer's charge per unit area is Q, while the voltage across the FE layer is Vf. The a0 and b0 coefficients are tied to the Landau parameters u, v, and w of the ferroelectric material, as well as the thickness of the material. Ferroelectric layer.

2tfu, 4tfv, 6tfw, a0 = 2tfu, b0 = 4tfv, c0 = 6tfw, u, v.

The higher-order terms in Eqs. (3) and (4) are not included inour analytical model.

The equation about φ0 (y) is expressed as

$$\frac{\partial^2\varphi_0(y)}{\partial y^2}=\frac{q}{\varepsilon_{si}}n_i\exp\left[\frac{\varphi_0(y)-V}{V_t}\right]. \quad (4)$$

φ0 (y) is solved using the following boundary conditions

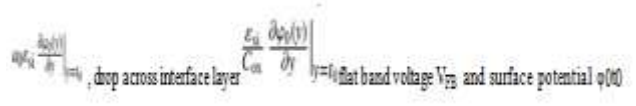
$$\left.\frac{\partial\varphi_0(y)}{\partial y}\right|_{y=0}=0, \quad (5)$$

$$V_{gs}-V_{FB}-\varphi_0(t_0)=\frac{\varepsilon_{si}}{C_{ox}}\left.\frac{\partial\varphi_0(y)}{\partial y}\right|_{y=t_0}+a_0\varepsilon_{si}\left.\frac{\partial\varphi_0(y)}{\partial y}\right|_{y=t_0}, \quad (6)$$

where $t_0$ = $t_{si}$/2. The boundary condition in Eq. (6) is derived from Kirchhoff's voltage law (KVL) along the gate-

*International Journal of Engineering Applied Sciences and Technology, 2022*
**Vol. 6, Issue 12, ISSN No. 2455-2143, Pages 241-246**
Published Online April 2022 in IJEAST (http://www.ijeast.com)

to-channel direction when the higher-order terms in Eq. (3) are ignored. To put it another way, the total applied gate voltage Vgs is equal to the sum of the drop across the ferroelectric layer.




$V_{FB} = \left(W_m - \chi - E_g/2\right)/q + V_t \ln\left(N_{CH}/n_i\right)$, where Wm is the gate metal's work function and χ and Eg are the Si channel's electron affinity and band gap, respectively. Using Eqs. (4) and (5) together, 0 (y) is expressed as

$$\varphi_0(y) = V + V_t \ln\left[\frac{B^2}{2\delta}\sec^2(By/t_0)\right], \qquad (7)$$

Except near the source junction, V remains constant (the value is equal to VDS) throughout the channel length direction (x). By combining Eqs. (7) and (6), the equation regarding B can be written as

$$\left(\frac{1}{C_{ox}} + a_0\right)\frac{2\varepsilon_{si}V_t}{t_0}B\tan(B) + V_t \ln\left[\frac{B^2}{2\delta}\sec^2(B)\right] = V_{gs} - V_{FB} - V, \qquad (8)$$

The flat-band voltage is VFB, and the insulator layer capacitance is Cox.
The 2D potential component 1 (x, y) of the Laplace equation can be determined using the separation of variables approach.

$$\varphi_1(x,y) = (a\exp(\lambda x/t_0) + b\exp(-\lambda x/t_0))\cos(\lambda y/t_0), \qquad (9)$$

where a and b are coefficients and λ is the eigen value.
Eqs. (10)– (13) are used to solve φ1 (x,y) in Eq. (9) using the boundary conditions.

$$\varphi_1(x,y)\big|_{x=0} = V_s - \varphi_0(y), \qquad (10)$$

$$\varphi_1(x,y)\big|_{x=L} = V_D - \varphi_0(y), \qquad (11)$$

$$-\varphi_1(x,t_0) = \frac{\varepsilon_{si}}{C_{ox}}\frac{\partial\varphi_1(x,y)}{\partial y}\bigg|_{y=t_0} + a_0\varepsilon_{si}\frac{\partial\varphi_1(x,y)}{\partial y}\bigg|_{y=t_0}. \qquad (12)$$

The source and drain potentials are VS = −Vtln (Ns/ni)VD = $V_{ds}$ + Vtln (ND/ $n_i$) respectively,
Combining Eq. (9) with Eq. (12), λ is expressed as

$$\lambda\tan(\lambda) = \frac{C_{ox}t_0}{\varepsilon_{si}(1 + a_0C_{ox})}. \qquad (13)$$

Using Fourier series solution, the parameters a and b obtained by Eq. (9) with Eq. (10) and (11) are expressed as

$$a = \frac{[V_D - V_S\exp(-\lambda L/t_0)]\sin(\lambda) - V_1[1 - \exp(-\lambda L/t_0)]}{[\lambda + 0.5\sin(2\lambda)]\sinh(\lambda L/t_0)}, \qquad (14)$$

$$b = \frac{-[V_D - V_S\exp(\lambda L/t_0)]\sin(\lambda) + V_1[1 - \exp(\lambda L/t_0)]}{[\lambda + 0.5\sin(2\lambda)]\sinh(\lambda L/t_0)}. \qquad (15)$$

The lateral and Vertical electric Fields for the DG TFETs are expressed has

$$E_x = -\partial\varphi_1(x,y)/\partial x = -[a\lambda/t_0\exp(\lambda x/t_0) - b\lambda/t_0\exp(-\lambda x/t_0)]\cos(\lambda y/t_0), \qquad (16)$$

$$E_y = -\partial\varphi_1(x,y)/\partial y - d\varphi_0(y)/dy = \lambda/t_0[a\exp(\lambda x/t_0) + b\lambda/t_0\exp(-\lambda x/t_0)]\sin(\lambda y/t_0) - 2BV_t\tan(By/t_0)/t_0. \qquad (17)$$

**Calculation of drain current**
The tunnelling current of the proposed device is computed analytically using Kane's model for the BTBT generation rate of carriers, which may be written as

$$I_{DS} = qt_sL_tW_{ch}A\bar{E}^{2.5}\exp\left(-\frac{B}{\bar{E}}\right), \qquad (18)$$

Wch is the proposed device's channel width, while A and B are the tunnelling parameters, which are $A=4.5*10^{14}$ $cm^{-12}$ $V^{-52}$ $s^{-1}$ and $B = 2*10^7$ V/cm, respectively. Furthermore, E = Eg/ (qLt) is the average electric field, and Lt is the shortest tunnelling length. The surface potential will reach Eg/q at the point Lt.
As a result, by plugging this value into Eq. (2), we can get the expression for Lt, which is written as

$$L_t = \frac{t_0}{\lambda}\ln\frac{\left[\left(V_s + E_g/q - \varphi_0(t_0)\right)/\cos\lambda\right] + \sqrt{\left[\left(V_s + E_g/q - \varphi_0(t_0)\right)/\cos\lambda\right]^2 - 4ab}}{2a}. \qquad (19)$$

*International Journal of Engineering Applied Sciences and Technology, 2022*
**Vol. 6, Issue 12, ISSN No. 2455-2143, Pages 241-246**
Published Online April 2022 in IJEAST (http://www.ijeast.com)

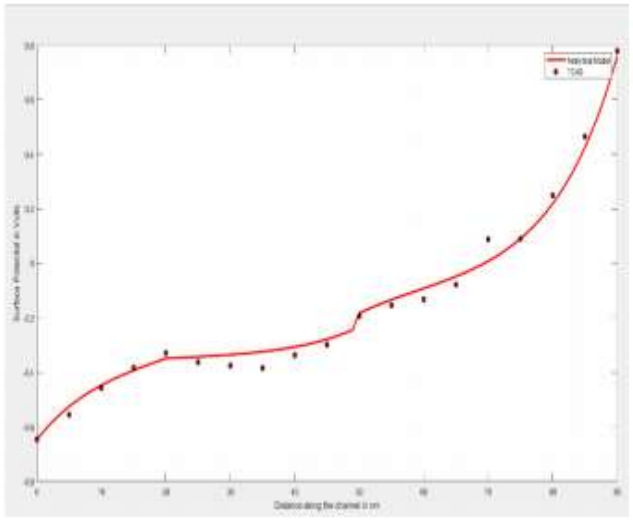


Fig. 3. Surface potential vs Distance along the channel in nm

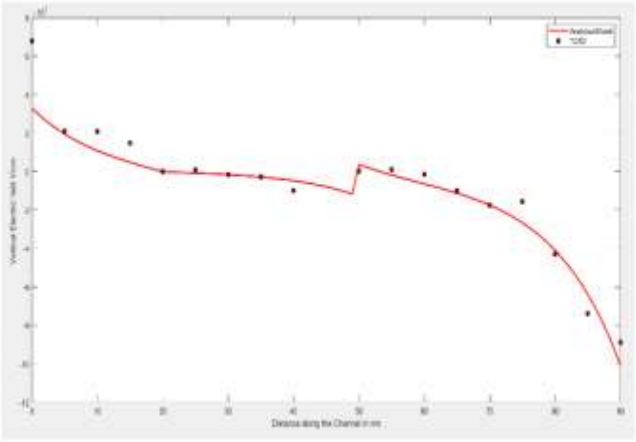


Fig.4. Vertical Electric Field vs Distance along the Channel innm on comparing the analytical model and Tcad software

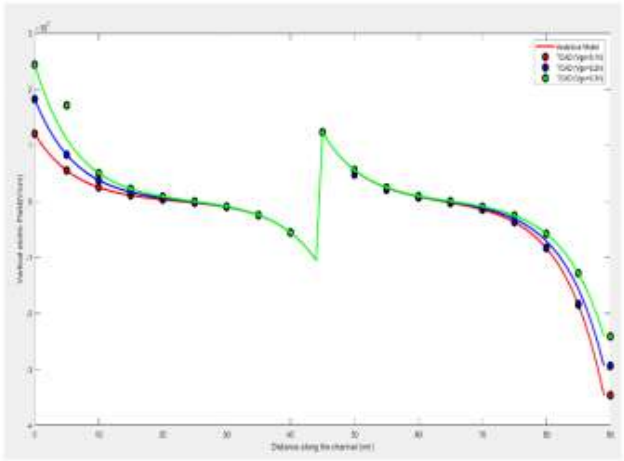


Fig 5. Vertical Electric Field vs Distance along thechannel at different Vgs Values

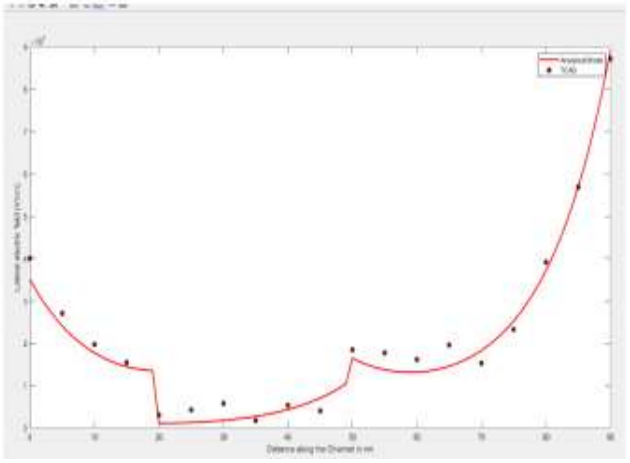


Fig.6. Lateral Field vs Distance along the Channel in nm

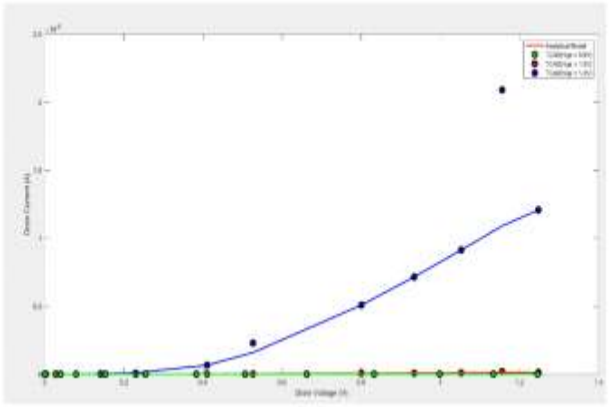


Fig 7. Drain Voltage vs Drain Current

## IV. RESULTS AND DISCUSSION

In this research, the TCAD device simulator Silvaco Atlas is used to test the non-local band-to-band tunnelling model (btbt), Lombardi mobility model (cvt), Shockley-Read-Hall recombination models (srh), and gap narrowing model (bgn). In addition, the effects of high dielectric constants, polarization, and hysteresis in ferroelectric materials were simulated using a Miller ferroelectric model. PZT residual polarization, saturation polarization of 0.6 C/cm2, and critical electrical field of 0.2 MV/cm are employed in the simulation. Remainder polarization, saturation polarization, and critical electrical polarization are all various thicknesses (such as 20, 15, and 10 nm of Si:HfO2). However, if establishing a link between ferroelectric material thickness and polarization and coercive field is challenging, it seems reasonable to explore the impact of ferroelectric material thickness on device performance under fixed polarization and coercive field conditions.

To put it another way, the effects of ferroelectric material thickness on polarization and the coercive field will not be considered.

For various Vgs, Figure 3 displays the surface potential of a DG TFET built of SBT material. The calculated and simulated outcomes are in perfect agreement. However, due to the analytical model's assumption of low voltage drop between the source and drain regions, certain errors can be seen at the source-channel and drain-channel junctions.
Figure 4 and 5 illustrates the vertical electric field for both simulation and analytical model.
Figure 6 depicts the lateral electric field for both the simulation and analytical model at Vgs = 1.5 V and Vds = 1.5
V. The double gate TFET produces a 27 percent improvement in the lateral electric field at the tunnel junction when compared to the traditional double gate TFET. The tunnellingenergy barrier width can be reduced as a result of the larger electric field at the tunnel junction, resulting in a higher on- current.
The OnOff current () ratio is an important metric to consider when building digital circuits. Ioff is defined as the drain current for Vgs = 0 V and Vds = 0.1.0 V in this study.
The voltage rises as the tf rises. Furthermore, the TFET with SBT material presented has the highest value. Choose one ofthe three materials for each tf, as shown in Fig.7.

## V. CONCLUSIONS

To explore device performances such as surface potential, electric field, shortest tunnelling length, on-state current, and on–off current ratio, an analytical model for the double gate TFET is built, taking into consideration the impacts of the channel mobile charge carriers. The potential model is also used in gate-all-around (GAA) TFETs, silicon-on-insulator (SOI) TFETs, and other device topologies. Furthermore, the on-state current of a double gate TFET grows in magnitude asthe thickness of the ferroelectric layer increases due to the shorter shortest tunnelling length. The effects of different ferroelectric material variants on on-state current and on–off current ratio have also been captured and explained; the results demonstrate that the SBT device has the highest on–state current and on–off current ratio. The study's findings urge further exploration and experimentation.

## VI. REFERENCES

[1] Prabhat V, Dutta A K. Analytical surface potential and drain current models of dual-metal-gate double-gate tunnel-FETs. IEEE Trans Electron Devices, 2016, 63(5): 2190.
[2] Mohammadi S, Khaveh H R T. An analytical model for double-gate tunnel FETs considering the junctions depletion regions and the channel mobile charge carriers. IEEE Trans Electron Devices, 2017, 64(3): 1268
[3] Nupur N, Abhinav K. Overcoming the drawback of lower sense margin in tunnel FET based dynamic memory along with enhanced charge retention and scalability. Nanotechnology, 2017, 28: 445203
[4] Kumar S, Goel E, Singh K, et al. A compact 2-D analytical model for electrical characteristics of double-gate tunnel field- effect transistors with a SiO2/high-k stacked gate-oxide structure. IEEE Trans Electron Devices, 2016, 63(8): 3291
[5] Navjeet B, Subir K S. An analytical model for tunnel barrier modulation in triple metal double gate TFET. IEEETrans Elec-tron Devices, 2015, 62(7): 2136
[6] Jiang C S, Liang R R, Xu J. Investigation of negative capacitance gate-all-around tunnel FETs combining numerical simulation and analytical modeling. IEEE Trans Nanotechnol,2017, 16(1): 58
[7] Chowdhury N, Azad S M F, Khosru Q D M. Negative capacitance tunnel field effect transistor: A novel device withlow sub- threshold swing and high on current. ECS Trans, 2014, 58(16): 1
[8] Hraziia, Vladimirescu A, Amara A, et al. An analysis on the ambipolar current in Si double-gate tunnel FETs. Solid-State Electron, 2012, 70(4): 67
[9] Wu J Z, Taur Y. Reduction of TFET OFF-current and sub- threshold swing by lightly doped drain. IEEE Trans Electron Devices, 2016, 63(8): 3342
[10] Wang Y B, Han G Q, Liu Y, et al. Investigation of GaAsBi/GaAsN type-II staggered heterojunction TFETs with the analytical model. IEEE Trans Electron Devices, 2017, 64(4): 1541
[11] Nigam K, Pandey S, Kondekar P N, et al. A barrier-controlled charge plasma-based TFET with gate engineering for ambipolar suppression and RF/linearity performance improvement. IEEE Trans Electron Devices, 2017, 64(6): 2751
[12] Xu H F, Guan B G. Two-dimensional analytical model for hetero-junction double-gate tunnel field-effect transistor with a stacked gate-oxide structure. Jpn J Appl Phys, 2017, 56(5): 054201
[13] Wang Y B, Han G Q, Liu Y, et al. Investigation of GaAsBi/GaAsN type-II staggered heterojunction TFETs with the analytical model. IEEE Trans Electron Devices, 2017, 64(4): 1541
[14] Bagga N, Dasgupta S. Surface potential and drain currentanalytical model of gate all around triple metal TFET. IEEE Trans Electron Devices, 2017, 64(2): 606
[15] Kondekar P N, Nigam K, Pandey S, et al. Design and analysis of polarity controlled electrically doped tunnel FET with bandgap engineering for analog/RF applications. IEEE Trans Electron Devices, 2017, 64(2): 412
[16] Ko E, Lee H, Park J D, et al. Vertical tunnel FET: design optimization with triple metal-gate layers. IEEE Trans Electron Devices, 2016, 63(12): 5030
[17] Girish P, Tapas D, Amit A, et al. Compact model for ferroelectric negative capacitance transistor with

MFIS structure.

[18] T. N. Theis and P. M. Solomon, "Its time to reinvent the transistor!" Science, vol. 327, no. 5973,pp. 1600–1601, 2010.

[19] In quest of the next switch prospects for greatly reduced power dissipation in a successor to the silicon field-effect transistor," Proceedings of theIEEE, vol. 98, no. 12, pp. 2005–2014, 2010.

[20] R. K. Cavin III, V. V. Zhirnov, J. A. Hutchby,and G. I. Bourianoff, "Energy barriers, demons, and minimum energy operation of electronic devices (plenary paper)," in SPIE Third International Symposium on Fluctuations and Noise. International Society for Optics and Photonics, 2005,pp.1–9.

[21] V. V. Zhirnov, R. K. Cavin, J. A. Hutchby, and G. I. Bourianoff, "Limits to binary logic switch scaling-a gedanken model," Proceedings of the IEEE,vol. 91, no. 11, pp. 1934–1939, 2003.

[22] S. Banerjee, W. Richardson, J. Coleman, and A. CHATTERJEE, "A new three-terminal tunnel device," IEEE electron device letters, vol. 8, n o. 8, pp.347–349, 1987.

[23] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," Nature, vol. 479, no. 7373, pp. 329–337, 2011.

[24] K. Gopalakrishnan, P. Griffin, and J. Plummer, "I-mos: a novel semiconductor device with a sub-threshold slope lower than kt/q," in Electron DevicesMeeting, 2002. IEDM '02. International, Dec 2002, pp. 289–292.

[25] H. Kam and T.-J. K. Liu, "Pull-in and release voltage design for nanoelectromechanical field-effect transistors," IEEE Transactions on Electron Devices, vol. 56, no. 12, pp. 3072–3082, 2009.

[26] M. Enachescu, M. Lefter, A. Bazigos, A. M. Ionescu, and S. D. Cotofana, "Ultra low power nem- fet based logic," in 2013 IEEE International Symposium on Circuits and Systems (ISCAS2013).IEEE, 2013, pp. 566–569.

[27] S. Salahuddin and S. Datta, "Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices," Nano Letters, vol. 8, no. 2, pp. 405–410, 2008, pMID: 18052402. [Online]. Available: http://dx.doi.org/10.1021/nl071804g

[28] K. M. Rabe, C. H. Ahn, and J. -M. Triscone, Physics of ferroelectrics: a modern perspective. Berlin, Germany: Springer Science & Business Media,2007, vol. 105.

[29] A. I. Khan, D. Bhowmik, P. Yu, S. J. Kim, X. Pan, R. Ramesh, and S. Salahuddin, "Experimen - tal evidence of ferroelectric negative capacitance in nanoscale heterostructures," Applied Physics Letters, vol. 99, no. 11, p. 113501, 2011.

[30] D. Jiménez, E. Miranda, and A. Godoy, "Analytic model for the surface potential and drain current in negative capacitance field-effect transistors," Electron Devices, IEEE Transactions on, vol. 57, no. 10, pp. 2405–2409, 2010.